# CMS80F752x Datasheet

## Enhanced Flash 8-Bit 1T 8051 Microcontrollers

## Rev. 0.5.2

# 1. Product Features

## 1.1 Features

- **Compatible with MCS-51 1T Instruction Set**
  - System clock frequency supports up to 48MHz
  - Fastest machine cycle: $1T_{SYS}$ @ $F_{SYS} \leq 24MHz$
  - Fastest machine cycle: $2T_{SYS}$ @ $F_{SYS} = 48MHz$
- **Memory**
  - Program FLASH: 32K×8Bit
  - Data FLASH: 1K×8Bit
  - Universal RAM: 256×8Bit
  - Universal XRAM: 2K×8Bit
  - Program FLASH supports partition protection and IAP functions
  - Data FLASH supports partition protection
- **3 Oscillation Modes**
  - HSI-internal high-speed oscillation: 48MHz
  - HSE-external high-speed oscillation: 8MHz/16MHz
  - LSI-internal low-speed oscillation: 32KHz
- **GPIO**
  - Up to 30 GPIOs
  - Supports pull-up/pull-down resistor function
  - Supports edge (rising edge/falling edge/both edges) interrupt
  - Supports wake-up function
- **Interrupt Sources**
  - Supports all external port interrupts
  - 4 timer interrupts
  - Other peripheral interrupts
- **Timers**
  - WDT Timer (Watch Dog Timer)
  - Timer0/1, Timer2
  - Timer5 (supports sleep wake-up function)
  - BRT (serial baud rate clock generator)
- **Cyclic Redundancy Check Unit**
  - CRC16 (CRC16-CCITT)
- **Enhanced PWM**
  - 6-channel enhanced PWM
  - 3 independent period counters
  - Supports independent/complementary/synchronous/group modes
  - Supports edge alignment
  - Supports complementary mode dead-time delay function
- **Communication Modules**
  - 1x SPI
  - 1x $I^2C$
  - 2x UART
  - UART1 can be mapped to any GPIO
- **Operating Voltage Range**
  - 2.5V to 5.5V
- **Operating Temperature Range**
  - -40℃ to 105℃
- **Low Voltage Reset (LVR)**
  - 2.5V/2.7V/3.0V/3.3V/3.7V/4.0V/4.3V
- **Low Voltage Detection (LVD)**
  - 2.5V/2.7V/3.0V/3.3V/3.7V/4.0V/4.3V
- **High-Precision 12-Bit ADC**
  - Up to 30 external AD channels
  - Selectable reference voltage (2.4V/VDD)
- **Hardware LED Dot Matrix Drive**
  - Fixed clock source
  - Supports cyclic scanning and interrupt scanning
  - Supports selectable data display for each light
  - Supports two selectable conduction times for each light
  - Supports up to 64 LEDs, configurable dot matrix options: 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8
- **Hardware LED Matrix Drive**
  - Selectable duty cycle: 1/4, 1/5, 1/6, 1/8
  - Supports both common cathode and common anode modes
  - Supports dimming mode with selectable dimming time
  - Fixed clock source
  - Selectable COM and SEG current
  - Supports up to: 4COM x 26SEG, 5COM x 25SEG 6COM x 24SEG, 8COM x 22SEG
- **High Sensitivity Touch**
- **Low Power Consumption Modes**
  - Idle Mode (IDLE)
  - Sleep Mode (STOP)
- **Supports 128-Bit Unique ID (UID)**
  - Each chip has a unique ID
- **Supports Two-wire Serial Programming and Debugging**

## 1.2 Product Comparison

| Peripheral interface \ Product model | | CMS80F7526 | CMS80F7528 | CMS80F7529 |
|---|---|---|---|---|
| Maximum clock frequency | | 48MHz | | |
| Memory module | APROM | 32 KB | | |
| | Data FLASH | 1 KB | | |
| | RAM | 256 B | | |
| | XRAM | 2 KB | | |
| Timer | WDT | 1 | | |
| | Timer0/1 | 2 (16-bit) | | |
| | Timer2 | 1 (16-bit) | | |
| | Timer5 | 1 (16-bit) | | |
| | BRT | 1 (10-bit) | | |
| Enhanced digital peripheral | CRC | CRC16-CCITT | | |
| | PWM | 6 (16-bit) | | |
| | LED matrix | 4COM x 14SEG<br>5COM x 13SEG<br>6COM x 12SEG<br>8COM x 10SEG | 4COM x 22SEG<br>5COM x 21SEG<br>6COM x 20SEG<br>8COM x 18SEG | 4COM x 26SEG<br>5COM x 25SEG<br>6COM x 24SEG<br>8COM x 22SEG |
| | LED dot-matrix | 4x4、5x5、6x6、6x7、7x7、7x8、8x8 | | |
| Communication module | SPI | 1 | | |
| | $I^2C$ | 1 | | |
| | UART | 2 | | |
| Analog module | 12-bit ADC (Number of external channels) | 18 | 26 | 30 |
| | Touch | 18 | 26 | 30 |
| GPIO | | 18 | 26 | 30 |
| LVR | | 2.5V/2.7V/3.0V/3.3V/3.7V/4.0V/4.3V | | |
| LVD | | 2.5V/2.7V/3.0V/3.3V/3.7V/4.0V/4.3V | | |
| Operating voltage | | 2.5~5.5V | | |
| Operating temperature | | -40~105℃ | | |
| Package | | SOP20 | SOP28 | LQFP32 |

# 2. System Overview

## 2.1 System Introduction

This series features an 8051 core, compatible with the MCS-51 1T instruction system. It is an 8-bit general-purpose I/O chip with a maximum operating frequency of 48MHz. The MCU has the following features:

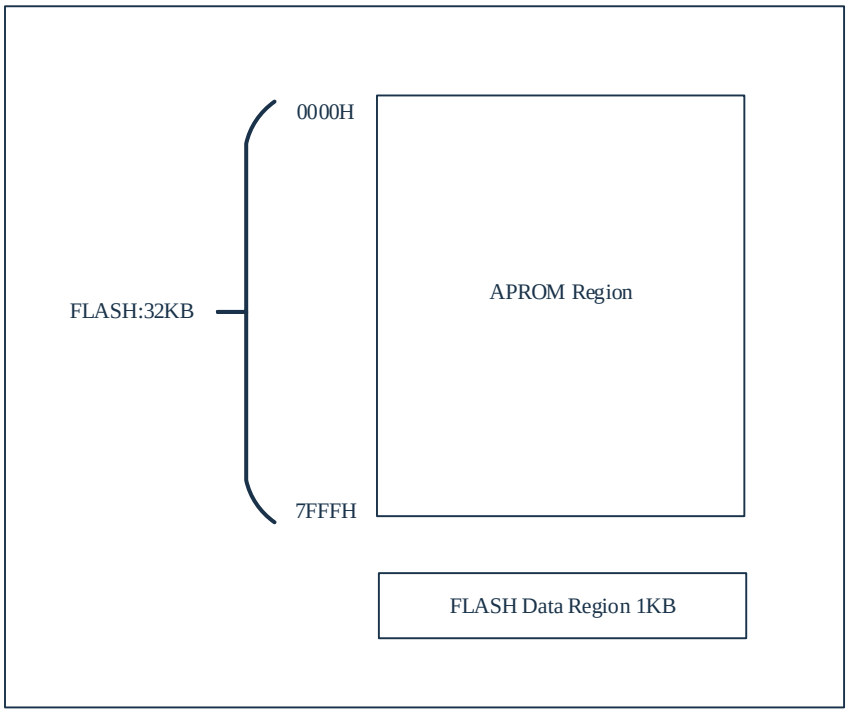
- It has a maximum of 32KB program memory, 256B RAM, 2KB XRAM, and 1KB non-volatile data memory.
- It supports three oscillation modes and external oscillator stop detection.
- It supports three working modes: normal, idle, and sleep, effectively reducing power consumption.
- Built-in low-voltage reset (LVR), low-voltage detection (LVD), and watch dog overflow reset protection features, enhancing system reliability.
- It has multiple interrupt sources, including external interrupts, timer interrupts, and peripheral interrupts, enabling timely response to external events and improving MCU utilization.
- It features six timers that support functions such as timing, counting, input capture, output compare, timer wake-up, and baud rate generation.
- It includes an enhanced PWM and a Cyclic Redundancy Check (CRC) unit.
- It supports up to 8 COM and 26 SEG LED driver modules.
- It offers six 16-bit PWM channels, supporting independent, complementary, and synchronous modes with dead-time control.
- It has one $I^2C$, one SPI, and two UART communication modules for data transfer between the system and other devices.
- It includes a high-precision 12-bit ADC with selectable internal reference voltage, up to 30 channels of high-sensitivity touch module, and an integrated temperature sensor, providing richer analog functionalities.

## 2.2 Memory Structure

### 2.2.1 Program Memory FLASH

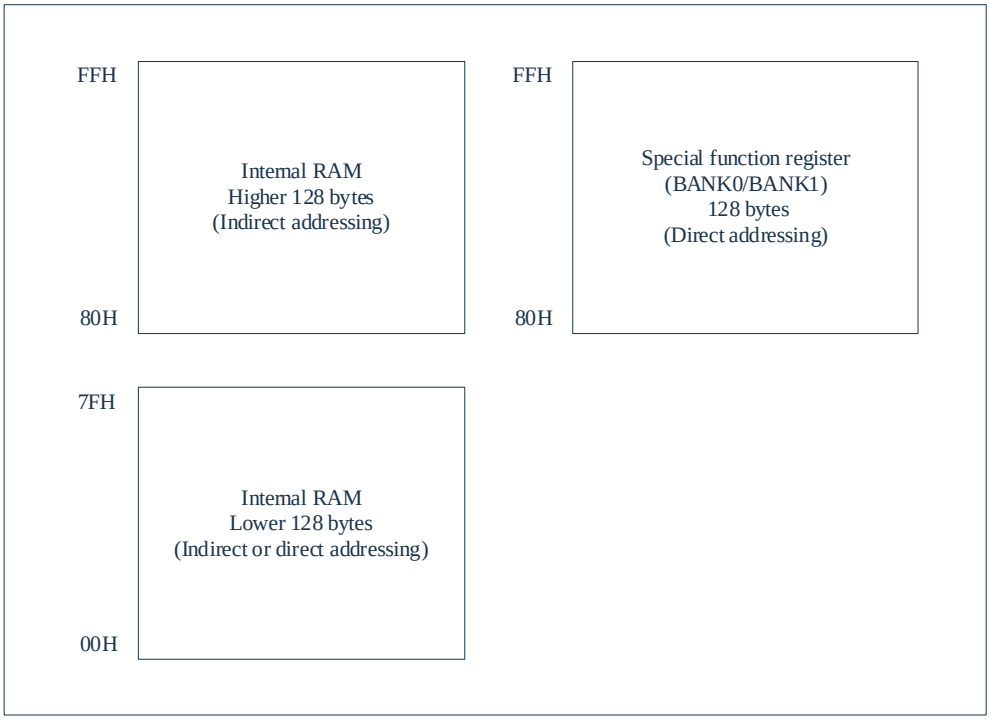
The chip features a 32KB FLASH memory space.

The memory space allocation structure block diagram is as follows:



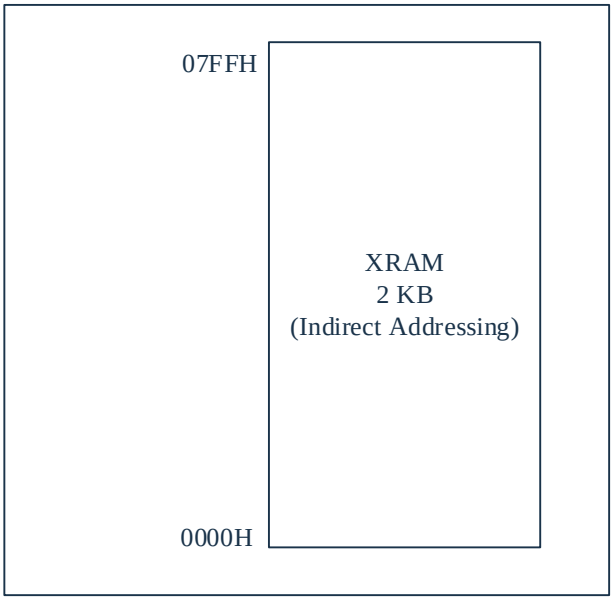
### 2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, and SFR. The structure diagram of RAM space allocation is shown in the figure below:



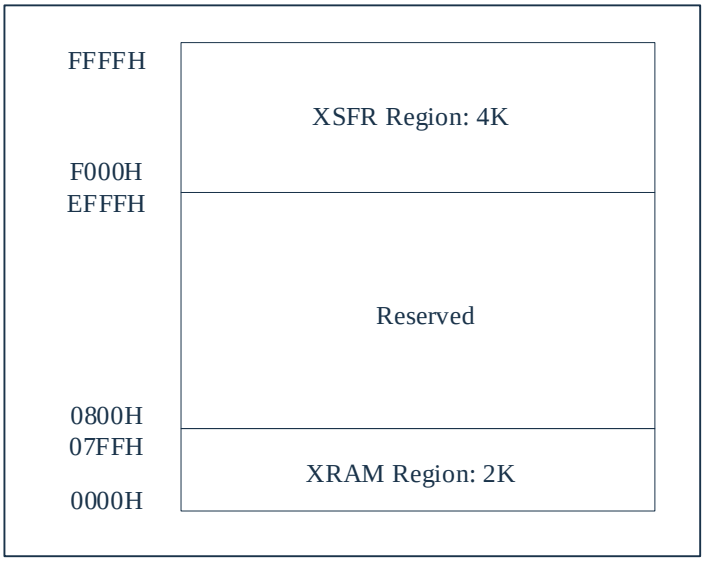

### 2.2.3 External Data Memory XRAM

The chip has a 2KB XRAM area, which is independent of the RAM/FLASH. The XRAM memory space allocation structure block diagram is shown below:



### 2.2.4 Special Function Register XSFR

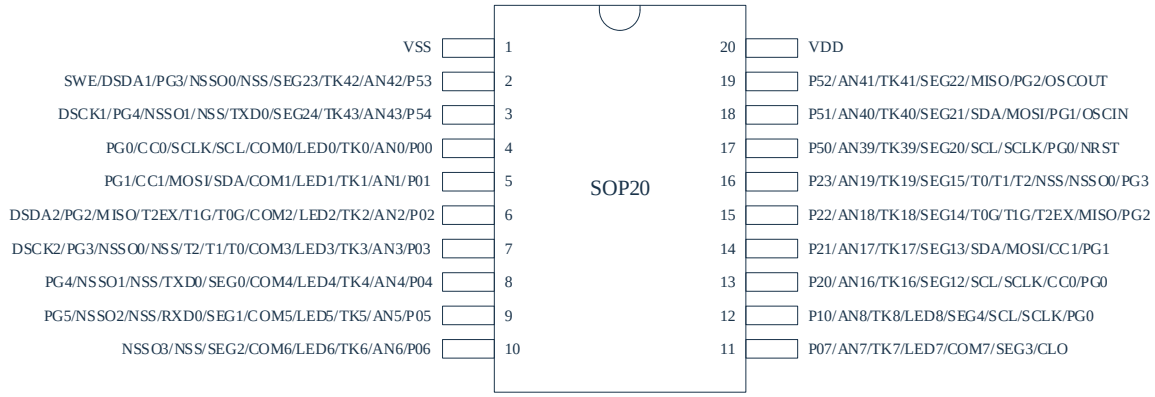
XSFR is a special register shared between the addressing space and XRAM, primarily including port control registers and other functional control registers. Its addressing range is as follows:



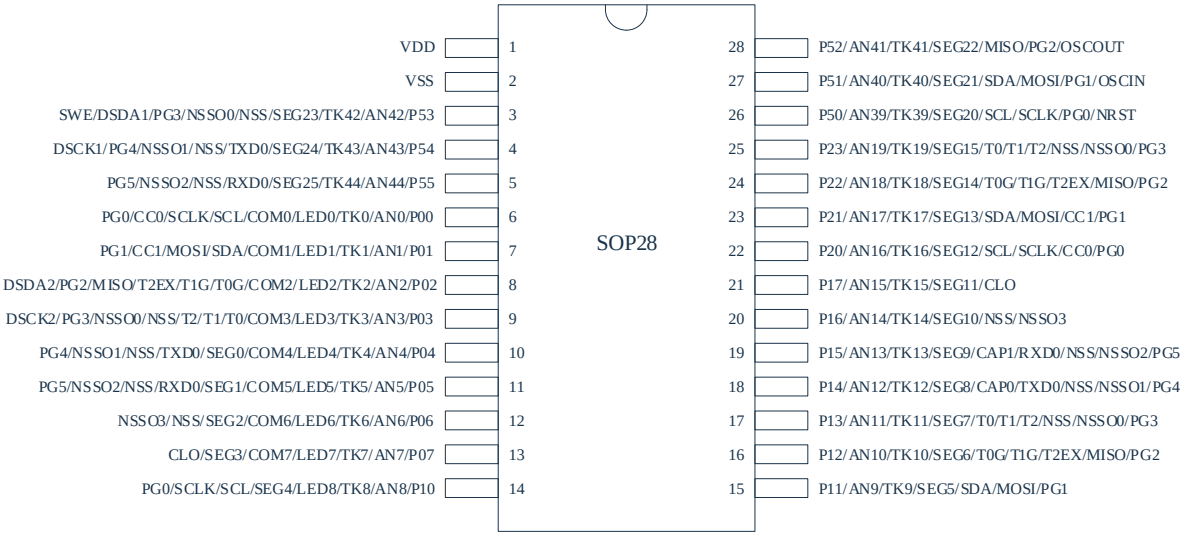
# 3. Pin Definition

## 3.1 Top View

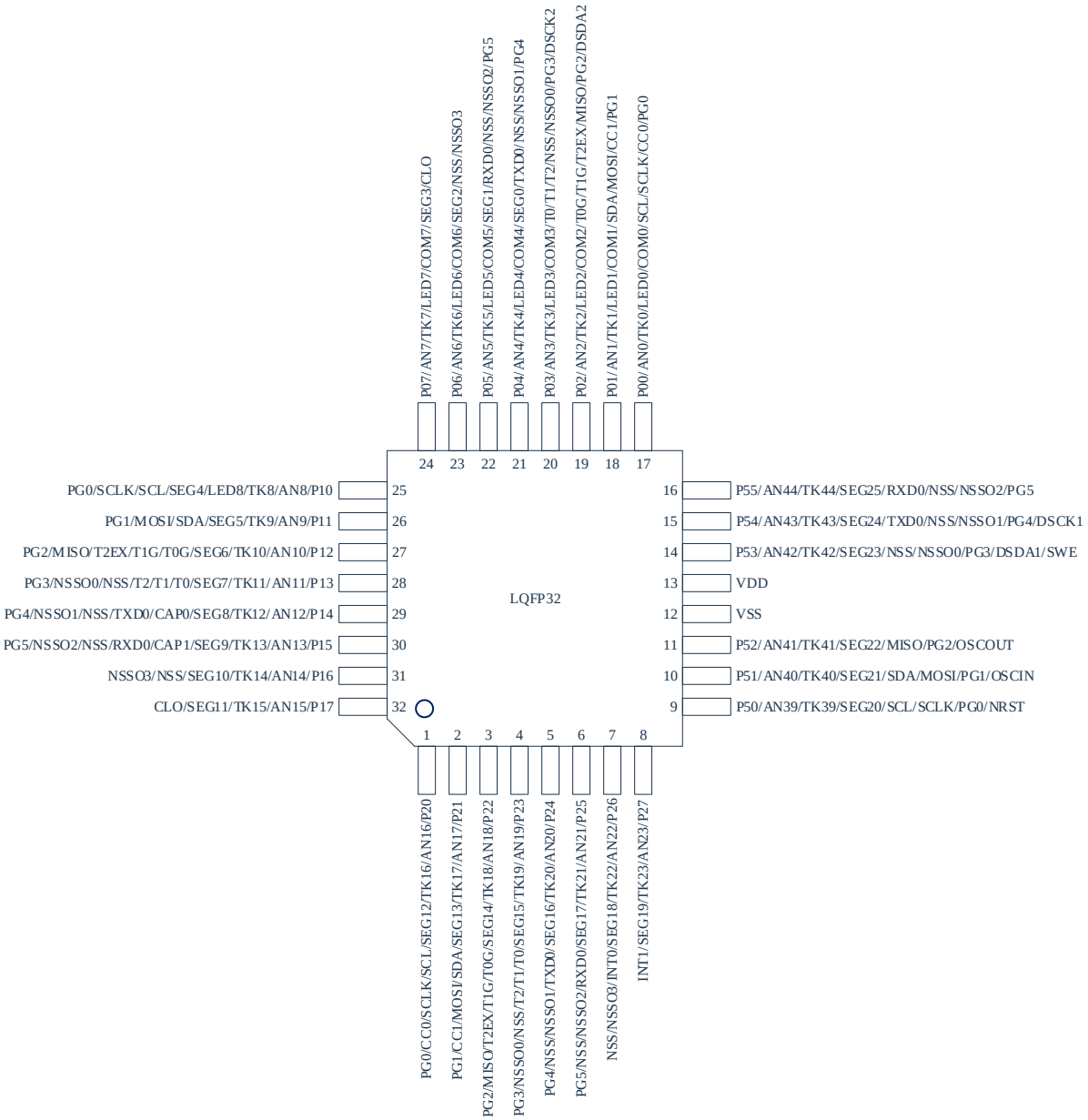
### 3.1.1 CMS80F7526




### 3.1.2 CMS80F7528



### 3.1.3 CMS80F7529



## 3.2 Pin Description

Symbol Explanation: I/O represents digital input/output, I represents digital input, O represents digital output, AI represents analog input, and AO represents analog output.

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| 4 | 6 | 17 | P00 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN0 | AI | ADC channel 0 input |
| | | | TK0 | AI | Touch key channel 0 input |
| | | | COM0 | O | LED COM0 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SCL | I/O | $I^2C$ clock input/output |
| | | | SCLK | I/O | SPI clock input/output |
| | | | CC0 | O | Timer2 compare output channel 0 |
| | | | PG0 | O | PWM channel 0 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 5 | 7 | 18 | P01 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN1 | AI | ADC channel 1 input |
| | | | TK1 | AI | Touch key channel 1 input |
| | | | COM1 | O | LED COM1 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SDA | I/O | $I^2C$ data input/output |
| | | | MOSI | I/O | SPI data master transmission/slave reception |
| | | | CC1 | O | Timer2 compare output channel 1 |
| | | | PG1 | O | PWM channel 1 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 6 | 8 | 19 | P02 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN2 | AI | ADC channel 2 input |
| | | | TK2 | AI | Touch key channel 2 input |
| | | | COM2 | O | LED COM2 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0G | I | Timer0 gate input |
| | | | T1G | I | Timer1 gate input |
| | | | T2EX | I | Timer2 falling edge auto-reload input |
| | | | MISO | I/O | SPI data master reception/slave transmission |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | PG2 | O | PWM channel 2 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| | | | DSDA2 | I/O | Programming data input/output |
| 7 | 9 | 20 | P03 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN3 | AI | ADC channel 3 input |
| | | | TK3 | AI | Touch key channel 3 input |
| | | | COM3 | O | LED COM3 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0 | I | Timer0 external clock input |
| | | | T1 | I | Timer1 external clock input |
| | | | T2 | I | Timer2 external event or gate input |
| | | | NSS0 | I/O | SPI slave chip select input/master chip select 0 output |
| | | | PG3 | O | PWM channel 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| | | | DSCK2 | I/O | Programming clock input |
| 8 | 10 | 21 | P04 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN4 | AI | ADC channel 4 input |
| | | | TK4 | AI | Touch key 4 channel |
| | | | SEG0 | O | LED SEG0 output |
| | | | COM4 | O | LED COM4 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | TXD0 | O | UART0 data output |
| | | | RXD0 | I | UART0 data input |
| | | | NSS1 | I/O | SPI slave chip select input/master chip select 1 output |
| | | | PG4 | O | PWM channel 4 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 9 | 11 | 22 | P05 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN5 | AI | ADC channel 5 input |
| | | | TK5 | AI | Touch key 5 channel |
| | | | SEG1 | O | LED SEG1 output |
| | | | COM5 | O | LED COM5 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | RXD0 | I | UART0 data input |
| | | | TXD0 | I | UART0 data output |
| | | | NSS2 | I/O | SPI slave chip select input/master chip select 2 output |
| | | | PG5 | O | PWM channel 5 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 10 | 12 | 23 | P06 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN6 | AI | ADC channel 6 input |
| | | | TK6 | AI | Touch key 6 channel |
| | | | SEG2 | O | LED SEG2 output |
| | | | COM6 | O | LED COM6 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | NSS3 | I/O | SPI slave chip select input/master chip select 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 11 | 13 | 24 | P07 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN7 | AI | ADC channel 7 input |
| | | | TK7 | AI | Touch key 7 channel |
| | | | SEG3 | O | LED SEG3 output |
| | | | COM7 | O | LED COM7 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | CLO | O | System clock divider output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 12 | 14 | 25 | P10 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN8 | AI | ADC channel 8 input |
| | | | TK8 | AI | Touch key 8 channel |
| | | | SEG4 | O | LED SEG4 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SCL | I/O | $I^2C$ clock input/output |
| | | | SCLK | I/O | SPI clock input/output |
| | | | PG0 | O | PWM channel 0 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 15 | 26 | P11 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | AN9 | AI | ADC channel 9 input |
| | | | TK9 | AI | Touch key 9 channel |
| | | | SEG5 | O | LED SEG5 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SDA | I/O | $I^2C$ data input/output |
| | | | MOSI | I/O | SPI data master transmission/slave reception |
| | | | PG1 | O | PWM channel 1 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 16 | 27 | P12 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN10 | AI | ADC channel 10 input |
| | | | TK10 | AI | Touch key 10 channel |
| | | | SEG6 | O | LED SEG6 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0G | I | Timer0 gate input |
| | | | T1G | I | Timer1 gate input |
| | | | T2EX | I | Timer2 falling edge auto-reload input |
| | | | MISO | I/O | SPI data master reception/slave transmission |
| | | | PG2 | O | PWM channel 2 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 17 | 28 | P13 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN11 | AI | ADC channel 11 input |
| | | | TK11 | AI | Touch key 11 channel |
| | | | SEG7 | O | LED SEG7 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0 | I | Timer0 external clock input |
| | | | T1 | I | Timer1 external clock input |
| | | | T2 | I | Timer2 external event or gate input |
| | | | NSS0 | I/O | SPI slave chip select input/master chip select 0 output |
| | | | PG3 | O | PWM channel 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 18 | 29 | P14 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN12 | AI | ADC channel 12 input |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | TK12 | AI | Touch key 12 channel |
| | | | SEG8 | O | LED SEG8 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | CAP0 | I | Timer2 input capture channel 0 |
| | | | TXD0 | O | UART0 data output |
| | | | RXD0 | I | UART0 data input |
| | | | NSS1 | I/O | SPI slave chip select input/master chip select 1 output |
| | | | PG4 | O | PWM channel 4 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 19 | 30 | P15 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN13 | AI | ADC channel 13 input |
| | | | TK13 | AI | Touch key 13 channel |
| | | | SEG9 | O | LED SEG9 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | CAP1 | I | Timer2 input capture channel 1 |
| | | | RXD0 | I | UART0 data input |
| | | | TXD0 | O | UART0 data output |
| | | | NSS2 | I/O | SPI slave chip select input/master chip select 2 output |
| | | | PG5 | O | PWM channel 5 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 20 | 31 | P16 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN14 | AI | ADC channel 14 input |
| | | | TK14 | AI | Touch key 14 channel |
| | | | SEG10 | O | LED SEG10 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | NSS3 | I/O | SPI slave chip select input/master chip select 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 21 | 32 | P17 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN15 | AI | ADC channel 15 input |
| | | | TK15 | AI | Touch key 15 channel |
| | | | SEG11 | O | LED SEG11 output |
| | | | EINT0 | I | External interrupt group EINT0 input |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | CLO | O | System clock divider output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 13 | 22 | 1 | P20 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN16 | AI | ADC channel 16 input |
| | | | TK16 | AI | Touch key 16 channel |
| | | | SEG12 | O | LED SEG12 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SCL | I/O | $I^2C$ clock input/output |
| | | | SCLK | I/O | SPI clock input/output |
| | | | CC0 | O | Timer2 compare output channel 0 |
| | | | PG0 | O | PWM channel 0 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 14 | 23 | 2 | P21 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN17 | AI | ADC channel 17 input |
| | | | TK17 | AI | Touch key 17 channel |
| | | | SEG13 | O | LED SEG13 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | SDA | I/O | $I^2C$ data input/output |
| | | | MOSI | I/O | SPI data master transmission/slave reception |
| | | | CC1 | O | Timer2 compare output channel 1 |
| | | | PG1 | O | PWM channel 1 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 15 | 24 | 3 | P22 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN18 | AI | ADC channel 18 input |
| | | | TK18 | AI | Touch key 18 channel |
| | | | SEG14 | O | LED SEG14 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0G | I | Timer0 gate input |
| | | | T1G | I | Timer1 gate input |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | T2EX | I | Timer2 falling edge auto-reload input |
| | | | MISO | I/O | SPI data master reception/slave transmission |
| | | | PG2 | O | PWM channel 2 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 16 | 25 | 4 | P23 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN19 | AI | ADC channel 19 input |
| | | | TK19 | AI | Touch key 19 channel |
| | | | SEG15 | O | LED SEG15 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | T0 | I | Timer0 external clock input |
| | | | T1 | I | Timer1 external clock input |
| | | | T2 | I | Timer2 external event or gate input |
| | | | NSS0 | I/O | SPI slave chip select input/master chip select 0 output |
| | | | PG3 | O | PWM channel 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | - | 5 | P24 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN20 | AI | ADC channel 20 input |
| | | | TK20 | AI | Touch key 20 channel |
| | | | SEG16 | O | LED SEG16 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | TXD0 | O | UART0 data output |
| | | | RXD0 | I | UART0 data input |
| | | | NSS1 | I/O | SPI slave chip select input/master chip select 1 output |
| | | | PG4 | O | PWM channel 4 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | - | 6 | P25 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN21 | AI | ADC channel 21 input |
| | | | TK21 | AI | Touch key 21 channel |
| | | | SEG17 | O | LED SEG17 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | RXD0 | I | UART0 data input |
| | | | TXD0 | O | UART0 data output |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | NSS2 | I/O | SPI slave chip select input/master chip select 2 output |
| | | | PG5 | O | PWM channel 5 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | - | 7 | P26 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN22 | AI | ADC channel 22 input |
| | | | TK22 | AI | Touch key 22 channel |
| | | | SEG18 | O | LED SEG18 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | INT0 | I | External interrupt 0 input |
| | | | NSS3 | I/O | SPI slave chip select input/master chip select 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | - | 8 | P27 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN23 | AI | ADC channel 23 input |
| | | | TK23 | AI | Touch key 23 channel |
| | | | SEG19 | O | LED SEG19 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | INT1 | I | External interrupt 1 input |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 17 | 26 | 9 | P50 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN39 | AI | ADC channel 39 input |
| | | | TK39 | AI | Touch key 39 channel |
| | | | SEG20 | O | LED SEG20 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | NRST | I | External reset input |
| | | | SCL | I/O | $I^2C$ clock input/output |
| | | | SCLK | I/O | SPI clock input/output |
| | | | PG0 | O | PWM channel 0 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 18 | 27 | 10 | P51 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN40 | AI | ADC channel 40 input |
| | | | TK40 | AI | Touch key 40 channel |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | SEG21 | O | LED SEG21 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | OSCIN | AI | External oscillation HSE input |
| | | | SDA | I/O | $I^2C$ data input/output |
| | | | MOSI | I/O | SPI data master transmission/slave reception |
| | | | PG1 | O | PWM channel 1 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 19 | 28 | 11 | P52 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN41 | AI | ADC channel 41 input |
| | | | TK41 | AI | Touch key 41 channel |
| | | | SEG22 | O | LED SEG22 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | OSCOUT | AO | External oscillation HSE output |
| | | | MISO | I/O | SPI data master reception/slave transmission |
| | | | PG2 | O | PWM channel 2 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 2 | 3 | 14 | P53 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN42 | AI | ADC channel 42 input |
| | | | TK42 | AI | Touch key 42 channel |
| | | | SEG23 | O | LED SEG23 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | DSDA1 | I/O | Programming/debugging data input/output |
| | | | SWE | I/O | Programming/debugging data and clock input/output |
| | | | NSS0 | I/O | SPI slave chip select input/master chip select 0 output |
| | | | PG3 | O | PWM channel 3 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 3 | 4 | 15 | P54 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN43 | AI | ADC channel 43 input |
| | | | TK43 | AI | Touch key 43 channel |
| | | | SEG24 | O | LED SEG24 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |

| Pin number | | | Pin name | Pin type | Description |
|---|---|---|---|---|---|
| SOP20 | SOP28 | LQFP32 | | | |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | DSCK1 | I | Programming/debugging clock input |
| | | | TXD0 | O | UART0 data output |
| | | | RXD0 | I | UART0 data input |
| | | | NSS1 | I/O | SPI slave chip select input/master chip select 1 output |
| | | | PG4 | O | PWM channel 4 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| - | 5 | 16 | P55 | I/O | GPIO is configured for input, output, pull-up, pull-down, and other functions through registers. |
| | | | AN44 | AI | ADC channel 44 input |
| | | | TK44 | AI | Touch key 44 channel |
| | | | SEG25 | O | LED SEG25 output |
| | | | EINT0 | I | External interrupt group EINT0 input |
| | | | EINT1 | I | External interrupt group EINT1 input |
| | | | EINT2 | I | External interrupt group EINT2 input |
| | | | EINT3 | I | External interrupt group EINT3 input |
| | | | RXD0 | I | UART0 data input |
| | | | TXD0 | O | UART0 data output |
| | | | NSS2 | I/O | SPI slave chip select input/master chip select 2 output |
| | | | PG5 | O | PWM channel 5 output |
| | | | TXD1 | O | UART1 data output |
| | | | RXD1 | I | UART1 data input |
| 20 | 1 | 13 | Power supply | P | Supply voltage input pin |
| 1 | 2 | 12 | Power supply | P | Ground pin |

Note: The debugging pins are DSDA1 (P53), DSCK1 (P54), or SWE (P53).

## 3.3 GPIO Features

The pins have multiple functions shared, and each I/O pin can be flexibly configured for digital or specified analog functions. As a GPIO, the I/O has the following features:

- The data latch status or pin status can be read.
- The external interrupt group can be configured to trigger interrupts on rising edge, falling edge, or both edges.
- The external interrupt group can be configured to wake up the chip on rising edge, falling edge, or both edge interrupts.
- It can be configured as a normal input, pull-up input, pull-down input, push-pull output, or open-drain output mode.

## 3.4 Pin Function List

Digital function port list:

| | External input | Digital function configuration | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
| P00 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SCL | SCLK | CC0 | PG0 | TXD1/RXD1 |
| P01 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SDA | MOSI | CC1 | PG1 | TXD1/RXD1 |
| P02 | T0G/T1G/T2EX EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | MISO | - | PG2 | TXD1/RXD1 |
| P03 | T0/T1/T2 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS0 | - | PG3 | TXD1/RXD1 |
| P04 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS1 | - | PG4 | TXD1/RXD1 |
| P05 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS2 | - | PG5 | TXD1/RXD1 |
| P06 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS3 | - | - | TXD1/RXD1 |
| P07 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | - | CLO | - | TXD1/RXD1 |
| P10 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SCL | SCLK | CLO | PG0 | TXD1/RXD1 |
| P11 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SDA | MOSI | - | PG1 | TXD1/RXD1 |
| P12 | T0G/T1G/T2EX EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | MISO | - | PG2 | TXD1/RXD1 |
| P13 | T0/T1/T2 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS0 | - | PG3 | TXD1/RXD1 |
| P14 | CAP0 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS1 | - | PG4 | TXD1/RXD1 |
| P15 | CAP1 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS2 | - | PG5 | TXD1/RXD1 |
| P16 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS3 | - | - | TXD1/RXD1 |
| P17 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | - | CLO | - | TXD1/RXD1 |
| P20 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SCL | SCLK | CC0 | PG0 | TXD1/RXD1 |
| P21 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SDA | MOSI | CC1 | PG1 | TXD1/RXD1 |
| P22 | T0G/T1G/T2EX EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | MISO | - | PG2 | TXD1/RXD1 |
| P23 | T0/T1/T2 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS0 | - | PG3 | TXD1/RXD1 |
| P24 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS1 | - | PG4 | TXD1/RXD1 |
| P25 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS2 | - | PG5 | TXD1/RXD1 |
| P26 | INT0 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS3 | - | - | TXD1/RXD1 |
| P27 | INT1 EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | - | | - | TXD1/RXD1 |
| P50 | NSRT EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SCL | SCLK | - | PG0 | TXD1/RXD1 |
| P51 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | SDA | MOSI | - | PG1 | TXD1/RXD1 |
| P52 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | MISO | - | PG2 | TXD1/RXD1 |
| P53 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | - | NSS0 | - | PG3 | TXD1/RXD1 |
| P54 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS1 | - | PG4 | TXD1/RXD1 |
| P55 | EINT0/EINT1/EINT2/EINT3 | GPIO | ANA | TXD0/ RXD0 | NSS2 | - | PG5 | TXD1/RXD1 |

List of LED ports, analog ports, CONFIG ports:

| | GPIO(0) | | | ANA(1) | | CONFIG |
|---|---|---|---|---|---|---|
| | LEDSEG | LEDCOM | LED dot matrix | ADC | TOUCH | |
| P00 | - | COM0 | LED0 | AN0 | TK0 | - |
| P01 | - | COM1 | LED1 | AN1 | TK1 | - |
| P02 | - | COM2 | LED2 | AN2 | TK2 | DSDA2 |
| P03 | - | COM3 | LED3 | AN3 | TK3 | DSCK2 |
| P04 | SEG0 | COM4 | LED4 | AN4 | TK4 | - |
| P05 | SEG1 | COM5 | LED5 | AN5 | TK5 | - |
| P06 | SEG2 | COM6 | LED6 | AN6 | TK6 | - |
| P07 | SEG3 | COM7 | LED7 | AN7 | TK7 | - |
| P10 | SEG4 | - | LED8 | AN8 | TK8 | - |
| P11 | SEG5 | - | - | AN9 | TK9 | - |
| P12 | SEG6 | - | - | AN10 | TK10 | - |
| P13 | SEG7 | - | - | AN11 | TK11 | - |
| P14 | SEG8 | - | - | AN12 | TK12 | - |
| P15 | SEG9 | - | - | AN13 | TK13 | - |
| P16 | SEG10 | - | - | AN14 | TK14 | - |
| P17 | SEG11 | - | - | AN15 | TK15 | - |
| P20 | SEG12 | - | - | AN16 | TK16 | - |
| P21 | SEG13 | - | - | AN17 | TK17 | - |
| P22 | SEG14 | - | - | AN18 | TK18 | - |
| P23 | SEG15 | - | - | AN19 | TK19 | - |
| P24 | SEG16 | - | - | AN20 | TK20 | - |
| P25 | SEG17 | - | - | AN21 | TK21 | - |
| P26 | SEG18 | - | - | AN22 | TK22 | - |
| P27 | SEG19 | - | - | AN23 | TK23 | - |
| P50 | SEG20 | - | - | AN39 | TK39 | NRST |
| P51 | SEG21 | - | - | AN40 | TK40 | OSCIN |
| P52 | SEG22 | - | - | AN41 | TK41 | OSCOUT |
| P53 | SEG23 | - | - | AN42 | TK42 | SWE/DSDA1 |
| P54 | SEG24 | - | - | AN43 | TK43 | DSCK1 |
| P55 | SEG25 | - | - | AN44 | TK44 | - |

Note: The chip pins are subject to the actual chip.

# 4. Function Summary

## 4.1 System Clock

The system clock has three clock sources, which can be selected through the system configuration register or user register settings for clock source and clock division. The system clock module has the following features:

- Internal high-speed oscillator (HSI) at 48MHz.
- External high-speed oscillator (HSE) at 8MHz/16MHz.
- Internal low-speed oscillator (LSI) at 32KHz.
- The external oscillator supports the Stop Mode Clock Monitoring (SCM) function when providing the system clock.

## 4.2 Reset

The reset operation is used to initialize the internal circuits of the chip, allowing the system to start working from a defined state. The chip supports the following types of reset:

- Power-on reset
- External reset
- Voltage detection reset
- Watch dog overflow reset
- Software reset

Each of these reset conditions requires a certain response time. The system provides a comprehensive reset process to ensure the reset operation is carried out smoothly.

## 4.3 Power Management

### 4.3.1 Operating Modes

The chip has three different operating modes to accommodate different power consumption requirements for various applications:

- Normal mode: The MCU is in normal operation, and peripherals are running as usual.
- Idle mode (IDLE): The MCU is in idle mode, where the CPU stops working while the peripherals continue to operate. This mode can be awakened by any interrupt.
- Sleep mode (STOP): The MCU is in sleep mode, where both the CPU and peripherals stop working. This mode can be awakened by INT0/1 interrupt, external interrupts, or a Timer5 interrupt.

### 4.3.2 Low Voltage Reset (LVR)

When the power supply voltage drops below the set detection voltage, the system will reset.

There are 7 selectable low voltage reset thresholds: 2.5V, 2.7V, 3.0V, 3.3V, 3.7V, 4.0V, and 4.3V.

### 4.3.3 Low Voltage Detection (LVD)

The low voltage detection circuit compares the power supply voltage with a set threshold voltage. If the power supply voltage falls below the set voltage, an interrupt request signal is generated.

The detection voltage range can be set from 2.5V to 4.3V, with 7 selectable levels.

## 4.4 Interrupt Control

The chip features multiple interrupt sources and interrupt vectors. Interrupts that can be configured by the user include INT0/1, Timer0/1, Timer2, Timer5, SCM, PWM, I2C, SPI, UART0/1, EINT0/1/2/3, ADC, LED, LVD, TOUCH. The actual number of interrupt sources varies by product.

The chip defines two interrupt priorities, allowing for two levels of interrupt nesting. When one interrupt is already being handled and a higher-priority interrupt request occurs, the higher-priority interrupt can preempt the current interrupt, allowing for interrupt nesting.

# 4.5 Timers

## 4.5.1 WDT

The Watch Dog Timer (WDT) is an on-chip timer that uses the system clock as its clock source. A WDT overflow will trigger a reset. The watch dog reset is a system protection feature that helps prevent the system from entering an indefinite deadlock state by resetting the system when it is in an unknown state. The WDT has the following features:

- 8 selectable overflow time intervals.
- Option to trigger a system reset on WDT overflow.

## 4.5.2 Timer0/1

Timer0 and Timer1 are similar in type and structure, both being 16-bit up-counters. Timer0 offers 4 operating modes, while Timer1 offers 3 operating modes, providing basic timing and event counting operations.

In timer mode, the timer register increments every 12 or 4 system cycles when the timer clock is enabled. In counter mode, the timer register increments whenever a falling edge is detected on the respective input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a regular timer.
- Can be used for gate timer functions.
- Can implement external counting functions.
- Can be used for gate counting functions.
- Provides counter overflow interrupts.

## 4.5.3 Timer2

Timer2 is a 16-bit timer that can be used for various digital signal generation and event capture, such as pulse generation, pulse-width modulation (PWM), and pulse width measurement. Timer2 has the following features:

- Can be used as a regular timer.
- Can be used for gate timer functions.
- Can implement external counting functions.
- Has reload disable, auto-reload on overflow, and auto-reload on external pin falling edge.
- Can trigger capture on rising edge, falling edge, both edges, or when writing to the lower byte of the capture register.
- Has a compare function, which can generate periodic signals and PWM waveforms with controllable duty cycles.
- Timer, external trigger, capture, and compare all can generate interrupts.

### 4.5.4 Timer5

Timer5 is a 16-bit timer, which, when using the LSI clock source, can be used to wake up the system from sleep mode. Timer5 has the following features:

- Timer function.
- Can set a 16-bit timer value.
- Can operate normally in sleep mode.
- Can generate an interrupt when the count value equals the timer value.
- Timer interrupt can wake up the system from idle or sleep mode.
- The counting clock can be selected from 1, 2, 4, 8, 16, 32, 64, or 128 prescalers.
- Clock source can be selected as LSI or Fsys.

### 4.5.5 Baud Rate Timer (BRT)

The BRT is a 10-bit baud rate timer, with its clock source coming from the system clock, mainly providing the clock for the UART module. BRT has the following features:

- Has an independent control switch.
- 10-bit incrementing count.

# 4.6 Enhanced Digital Peripherals

## 4.6.1 Cyclic Redundancy Check (CRC) Unit

Cyclic Redundancy Check (CRC) is one of the most commonly used error-checking codes in the field of data communication. Its feature is that the lengths of both the information field and the check field can be chosen arbitrarily. The chip's CRC check unit uses the polynomial "$X^{16}+X^{12}+X^5+1$" (CRC16-CCITT). Through programming, the data to be checked can be specified, making this module applicable not only to the code flash area but also for multi-purpose checks.

## 4.6.2 Enhanced PWM Module

The enhanced PWM module supports 6 PWM generators, where the period and duty cycle can be set independently. PWM features the following:

- Supports two waveform output modes: one-shot and continuous.
- Supports four control modes: independent, complementary, synchronized, and group control.
- The counting clock can be divided by factors of 1, 2, 4, 8, 16, 32, 64, or 128.
- Supports edge-alignment.
- Supports dead-time programming.
- Output polarity can be set.
- Supports down-count comparison and zero-crossing interrupt.

# 4.7 Display Interfaces

## 4.7.1 Hardware LED Dot Matrix Driver Module

The LED dot matrix driver module facilitates the driving of LED dot matrix displays. This module has the following features:

- Fixed clock source.
- Supports cyclic scanning and interrupt scanning.
- Supports selectable data display for each LED.
- Supports two selectable conduction times for each LED.
- Supports up to 64 LED driving with configurable matrix options: 4x4, 5x5, 6x6, 6x7, 7x7, 7x8, 8x8.

## 4.7.2 Hardware LED Matrix Driver Module

The LED matrix driver module facilitates the driving of LED matrix displays. This module has the following features:

- Four duty cycles available: 1/4, 1/5, 1/6, and 1/8.
- Fixed clock source.
- Supports both common cathode and common anode driving modes for the COM port.
- Supports up to 8 COM ports and 26 SEG ports.
- Each COM/SEG port has an enable control bit.
- COM port current options: 55mA and 220mA.
- SEG port current options with 16 levels, maximum current up to 50mA.
- Supports dimming mode with selectable dimming time.

# 4.8 Communication Modules

## 4.8.1 SPI Module

SPI (Serial Peripheral Interface) is a fully configurable SPI master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI enables MCU communication with serial peripheral devices and also allows processor-to-processor communication in a multi-master system. The SPI module has the following features:

- Full-duplex synchronous serial data transfer.
- Supports master/slave mode.
- Supports multi-master systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock ($F_{SYS} \leq 24MHz$).
- Bit rates derived from system clock at 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512.
- Supports four different transfer formats.
- Interrupt generation upon completion of transmission/reception.

## 4.8.2 I²C Module

The I²C two-wire bidirectional serial bus controller provides a simple and efficient connection for data exchange between microprocessors and the I²C bus. The I²C module has the following features:

- Supports master/slave mode.
- Bidirectional data transfer between master and slave.
- Performs arbitration and clock synchronization.
- Supports multi-master systems.
- Arbitration for simultaneous data transfer between multiple masters, avoiding serial data corruption on the bus.
- The bus uses serial synchronized clock, enabling devices to transmit at different rates.
- Programmable clock for multiple rate control.
- Supports 7-bit/10-bit slave address modes.

## 4.8.3 UARTn Module

The UARTn module includes two serial ports, UART0 and UART1, which have identical functions. The UARTn module has the following features:

- Full-duplex serial port.
- Supports variable baud rate in 8-bit asynchronous transmit/receive mode.
- Supports variable baud rate in 9-bit asynchronous transmit/receive mode.
- Baud rate can be generated by Timer1/BRT module.
- Interrupt generation upon completion of transmission/reception.

# 4.9 Analog Modules

## 4.9.1 Analog-to-Digital Converter (ADC)

The ADC module is a 12-bit successive approximation analog-to-digital converter. The analog input signal from the port is routed through a multiplexer before being connected to the input of the ADC. The ADC generates a 12-bit binary result based on the input analog signal and stores the result in the ADC result register. The ADC has the following features:

- Supports up to 30 external channels.
- The ADC conversion clock has 8 selectable clock frequencies.
- The ADC reference voltage can be selected as VDD/2.4V.
- A complete 12-bit conversion requires 18.5 ADC conversion cycles.
- Supports generating an interrupt upon ADC conversion completion.

## 4.9.2 Touch Module (TOUCH)

The touch module is an integrated circuit designed for implementing human touch interfaces, replacing mechanical touch buttons. It provides a waterproof, dustproof, sealed, rugged and aesthetically pleasing operating interface.

Technical Parameters:

- Supports up to 30 selectable touch buttons.
- No external touch capacitor is required.

## 4.10 Flash Memory

The FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH). Access operations to these memories are performed through the related special function registers (SFR) to enable In-Application Programming (IAP). The FLASH memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Page erase operation.
- FLASH space CRC operation.

## 4.11 Unique ID (UID)

Each chip has a unique 128-bit identification number, known as the Unique ID (UID). It is set at the factory and cannot be modified by the user.

The address of the UID is located from 0x680 to 0x68F, corresponding to 16 bytes.

# 5. User Configuration

The System Configuration Register (CONFIG) is a FLASH option for the MCU's initial conditions, and the program cannot access or modify it. The following settings can be configured through the system configuration register:

- Watch dog operation mode.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low-voltage reset voltage.
- Debug mode enable or disable.
- Oscillation mode and prescaler selection.
- Internal high-speed oscillator prescaler selection.
- External reset configuration and port selection.
- Sleep wake-up wait time.

# 6. Electrical Characteristics

Unless otherwise specified, the temperature condition for the following parameters is $T_A$ = 25℃.

## 6.1 Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{ST}$ | Storage temperature | -55 | 150 | ℃ |
| $T_A$ | Operating temperature | -40 | 105 | ℃ |
| VDD-VSS | Supply voltage | -0.3 | 5.8 | V |
| $V_{IN}$ | Input voltage | VSS-0.3 | VDD+0.3 | V |
| $I_{DD}$ | VDD maximum input current | - | 250 | mA |
| $I_{SS}$ | VSS maximum output current | - | 300 | mA |
| $I_{IO}$ | Single IO maximum sink current | - | 55 | mA |
| | Single IO maximum sink current (LED_COM) | - | 220 | mA |
| | Single IO maximum source current | - | 50 | mA |
| | Single IO maximum source current (LED_SEG) | - | 50 | mA |
| | All IO maximum sink current | - | 250 | mA |
| | All IO maximum source current | - | 200 | mA |

Note: If the operating conditions of the device exceed the range of **Absolute Maximum Ratings**, it will cause permanent damage to the device. The functionality can be guaranteed only when the device works within the scope specified in the manual. Operating the chip under absolute maximum rating conditions may affect the device's reliability.

## 6.2 DC Electrical Characteristics

VDD-VSS=2.5～5.5V, $T_A$=25℃

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD | Operating voltage | $F_{SYS}$=48MHz, machine cycle=2T<br>$F_{SYS}$=8MHz~24MHz, machine cycle=1T | 2.5 | - | 5.5 | V |
| | | Touch module operating voltage range | 3.5 | - | 5.5 | V |
| $I_{DD}$ | Normal mode | VDD=5V, $F_{SYS}$=48MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$/2 | - | 8 | - | mA |
| | | VDD=3V, $F_{SYS}$=48MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$/2 | - | 8 | - | mA |
| | | VDD=5V, $F_{SYS}$=24MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 5 | - | mA |
| | | VDD=3V, $F_{SYS}$=24MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 5 | - | mA |
| | | VDD=5V, $F_{SYS}$=16MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 4 | - | mA |
| | | VDD=3V, $F_{SYS}$=16MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 4 | - | mA |
| | | VDD=5V, $F_{SYS}$=8MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 3 | - | mA |
| | | VDD=3V, $F_{SYS}$=8MHz, all peripherals OFF<br>$F_{CPU}$=$F_{SYS}$ | - | 3 | - | mA |
| | IDLE mode | VDD=5V, $F_{SYS}$=48MHz, all peripherals OFF | - | 7 | - | mA |
| | | VDD=3V, $F_{SYS}$=48MHz, all peripherals OFF | - | 7 | - | mA |
| | | VDD=5V, $F_{SYS}$=24MHz, all peripherals OFF | - | 4 | - | mA |
| | | VDD=3V, $F_{SYS}$=24MHz, all peripherals OFF | - | 4 | - | mA |
| | | VDD=5V, $F_{SYS}$=16MHz, all peripherals OFF | - | 3.5 | - | mA |
| | | VDD=3V, $F_{SYS}$=16MHz, all peripherals OFF | - | 3.5 | - | mA |
| | | VDD=5V, $F_{SYS}$=8MHz, all peripherals OFF | - | 2.5 | - | mA |
| | | VDD=3V, $F_{SYS}$=8MHz, all peripherals OFF | - | 2.5 | - | mA |
| $I_{SLEEP1}$ | Sleep current | VDD=3V, all peripherals OFF, LSI, Timer5 enabled | - | 7 | - | uA |
| $I_{SLEEP2}$ | Sleep current | VDD=3V, all peripherals OFF | - | 6 | - | uA |
| $I_{LI}$ | Input leakage | - | -1 | - | 1 | uA |
| $V_{IL}$ | Input voltage, low | - | VSS | - | 0.3VDD | V |
| $V_{IH}$ | Input voltage, high | - | 0.7VDD | - | VDD | V |
| $V_{OL}$ | Output voltage, low | VDD=5V, $I_{OL1}$=58.9mA | - | - | 1.5 | V |
| | | VDD=5V, $I_{OL2}$=225mA (LED COM) | - | - | 1.5 | V |
| | | VDD=3V, $I_{OL1}$=26mA | - | - | 0.9 | V |
| | | VDD=3V, $I_{OL2}$=100mA (LED COM) | - | - | 0.9 | V |
| $V_{OH}$ | Output voltage, high | VDD=5V, $I_{OH1}$=54.8mA | 3.5 | - | - | V |
| | | VDD=5V, $I_{OH2}$=54.2mA (LED SEG Max) | 3.5 | - | - | V |
| | | VDD=5V, $I_{OH3}$=6.3mA (LED SEG Min) | 3.5 | - | - | V |
| | | VDD=3V, $I_{OH1}$=23.9mA | 2.1 | - | - | V |
| | | VDD=3V, $I_{OH2}$=23.7mA (LED SEG Max) | 2.1 | - | - | V |
| | | VDD=3V, $I_{OH3}$=2.6mA (LED SEG Min) | 2.1 | - | - | V |
| $R_{PH}$ | Pull-up resistor | - | - | 30 | - | KΩ |
| $R_{PL}$ | Pull-down resistor | - | - | 30 | - | KΩ |

# 6.3 AC Electrical Parameters

## 6.3.1 Power-on/Power-off Operation

$T_A$=25℃

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{RESET}$ | Reset time | VDD=5V | - | 22 | - | ms |
| TVDDR | VDD rise rate | VDD=5V | 20 | - | - | us/V |
| TVDDF | VDD fall rate | VDD=5V | 20 | - | - | us/V |

Remark: This specification is guaranteed by the design, and is not tested in mass production.

## 6.3.2 External Oscillator

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{HSE}$ | Operating voltage | F=8/16MHz, $C_{XT}$=5-20pF | 2.5 | - | 5.5 | V |

## 6.3.3 Internal Oscillator

VDD=2.5V-5.5V

| Symbol | Parameter | Test condition | Frequency error | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $F_{HSI}$ | Internal high-speed 48MHz | $T_A$=25℃ | ±1% | | 48 | | MHz |
| | | $T_A$=-20℃ to 85℃ | ±2% | | 48 | | MHz |
| | | $T_A$=-40℃ to 105℃ | ±3% | | 48 | | MHz |
| $F_{LSI}$ | Internal low-speed 32KHz | $T_A$=25℃ | ±20% | - | 32 | - | KHz |
| | | $T_A$=-40℃ to 105℃ | ±50% | - | 32 | - | KHz |

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

## 6.3.4 POR Electrical Parameters

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Low power reset detection circuit | $T_A$=25℃ | | 2.1 | | V |

Remark: This specification is guaranteed by the design, and is not tested in mass production.

## 6.3.5 LVD Electrical Parameters

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{LVR1}$ | Low voltage detection threshold 2.50V | 2.35 | 2.5 | 2.65 | V |
| $V_{LVR2}$ | Low voltage detection threshold 2.70V | 2.55 | 2.7 | 2.85 | V |
| $V_{LVR3}$ | Low voltage detection threshold 3.00V | 2.85 | 3.0 | 3.15 | V |
| $V_{LVR4}$ | Low voltage detection threshold 3.30V | 3.15 | 3.3 | 3.45 | V |
| $V_{LVR5}$ | Low voltage detection threshold 3.70V | 3.55 | 3.7 | 3.85 | V |
| $V_{LVR6}$ | Low voltage detection threshold 4.00V | 3.85 | 4.0 | 4.15 | V |
| $V_{LVR7}$ | Low voltage detection threshold 4.30V | 4.15 | 4.3 | 4.45 | V |

### 6.3.6 LVD Electrical Parameters

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{LVD1}$ | Low voltage detection threshold 2.50V | 2.35 | 2.5 | 2.65 | V |
| $V_{LVD2}$ | Low voltage detection threshold 2.70V | 2.55 | 2.7 | 2.85 | V |
| $V_{LVD3}$ | Low voltage detection threshold 3.00V | 2.85 | 3.0 | 3.15 | V |
| $V_{LVD4}$ | Low voltage detection threshold 3.30V | 3.15 | 3.3 | 3.45 | V |
| $V_{LVD5}$ | Low voltage detection threshold 3.70V | 3.55 | 3.7 | 3.85 | V |
| $V_{LVD6}$ | Low voltage detection threshold 4.00V | 3.85 | 4.0 | 4.15 | V |
| $V_{LVD7}$ | Low voltage detection threshold 4.30V | 4.15 | 4.3 | 4.45 | V |

## 6.4 Flash Electrical Parameters

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_F$ | FLASH operating voltage | - | 2.5 | - | 5.5 | V |
| $T_F$ | FLASH operating temperature | - | -40 | 25 | 105 | ℃ |
| $N_{ENDURANCE}$ | Erase cycle count[Note 1] | Program FLASH | 20,000 | - | - | Cycle |
| | | Data FLASH | 100,000 | - | - | Cycle |
| $T_{RET}$ | Data retention time[Note 1] | 25℃ | 100 | - | - | year |
| $T_{ERASE}$ | Sector erase time | - | - | 1.5 | - | ms |
| $T_{WRITE}$ | Write time | - | - | 30 | - | us |
| $T_{READ}$ | Read time | - | - | 3*Tsys | - | - |
| $I_{DD1}$ | Read current | - | - | - | 2.5 | mA |
| $I_{DD2}$ | Programming current | - | - | - | 3.6 | mA |
| $I_{DD3}$ | Erase current | - | - | - | 2 | mA |

Note 1: This specification is guaranteed by the design, and is not tested in mass production.

# 6.5 Analog Characteristics

## 6.5.1 BANDGAP Electrical Characteristics

$T_A$=25℃

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{BG}$ | Internal reference 0.8V | VDD=2.5~5.5V, $T_A$=25℃ | 0.792 | 0.8 | 0.808 | V |
| | | VDD=2.5~5.5V, $T_A$=-20℃ to 85℃ | 0.788 | 0.8 | 0.812 | V |
| | | VDD=2.5~5.5V, $T_A$=-40℃ to 105℃ | 0.784 | 0.8 | 0.816 | V |

## 6.5.2 Internal Reference Voltage 2.4V Electrical Characteristics

$T_A$=25℃

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCLDO}$ | 2.4V | VDD=2.9~5.5V, $T_A$=25℃ | 2.376 | 2.4 | 2.424 | V |
| | | VDD=2.9~5.5V, $T_A$=-20℃ to 85℃ | 2.364 | 2.4 | 2.436 | V |
| | | VDD=2.9~5.5V, $T_A$=-40℃ to 105℃ | 2.352 | 2.4 | 2.448 | V |

## 6.5.3 ADC Electrical Characteristics

$T_A$=25℃

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{AVDD}$ | ADC operating voltage | | 2.5 | - | 5.5 | V |
| $V_{REF1}$ | Reference voltage 1 | | - | $V_{AVDD}$ | - | V |
| $V_{REF2}$ | Reference voltage 2(Note 1) | | 2.385 | 2.4 | 2.415 | V |
| $V_{ADI}$ | Input voltage | | 0 | - | $V_{REF}$ | V |
| $N_R$ | Resolution | | | 12 | | Bit |
| DNL | Differential nonlinearity error ($V_{REF}$=$V_{AVDD}$=5V, $T_{ADCK}$=0.5us) | | | ±2 | | LSB |
| INL | Integral nonlinearity error ($V_{REF}$=$V_{AVDD}$=5V, $T_{ADCK}$=0.5us) | | | ±4 | | LSB |
| $T_{ADCK}$ | ADC clock cycle | $V_{REF}$=VDD=5V | 0.5 | - | - | us |
| | | $V_{REF}$=$V_{REF2}$ | 2 | - | - | us |
| $T_{ADC}$ | ADC conversion time | | - | 18.5 | - | $T_{ADCK}$ |
| $F_S$ | Sampling rate ($V_{REF}$=$V_{AVDD}$=5V) | | | 100 | | Ksps |

Note: When $V_{REF}$ =$V_{REF2}$, the precision is 8 bits.

Note 1: Test conditions: $T_A$ = 25℃ and $V_{AVDD}$ = 5.0V.

# 6.6 EMC Characteristics

## 6.6.1 EFT Electrical Characteristics

| Symbol | Parameter | Test condition | Grade |
|---|---|---|---|
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 0.1uF (capacitance) on VDD and VSS pins to induce a functional disturbance | $T_A$ = + 25℃, $F_{SYS}$=48MHz, conforms to IEC 61000-4-4 | 4B |

Note: The electrical fast transient burst (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.) The EFT parameters in the above table are the results measured on the internal test platform of the CMS, and are not applicable to all application environments. The test data is only for reference. All aspects of system design may affect the EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting the system operation as much as possible. It is recommended to analyze the interference path and optimize the design to achieve the best anti-interference performance.

## 6.6.2 ESD Electrical Characteristics

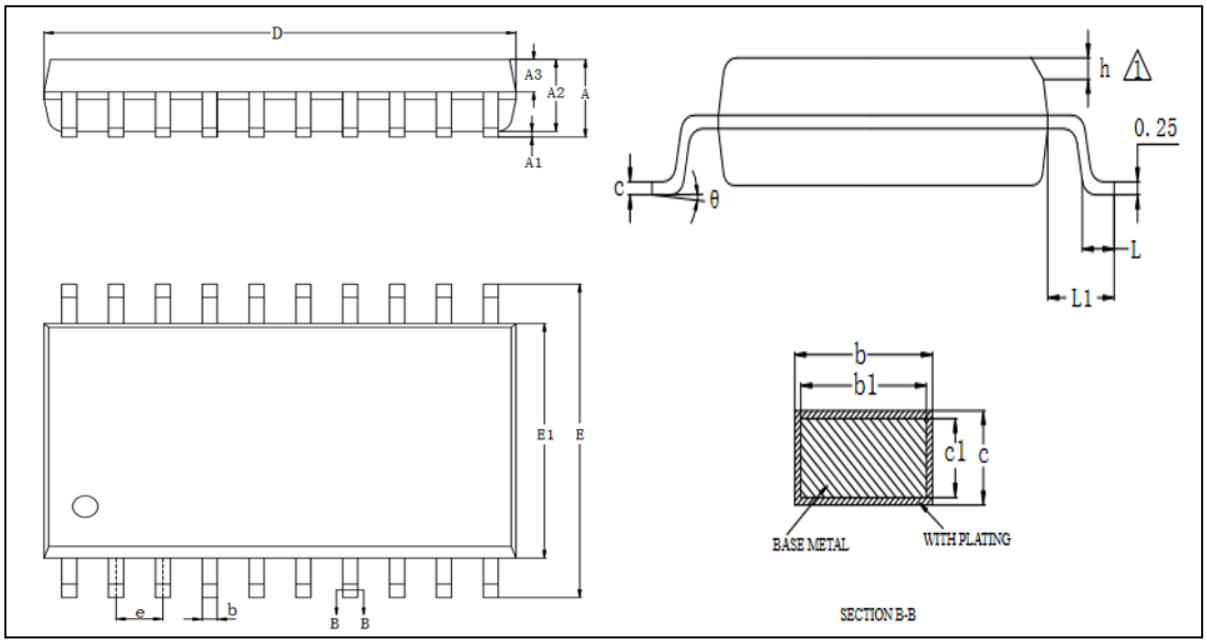
| Symbol | Parameter | Test condition | Grade |
|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge (Human body discharge mode HBM) | TA = 25℃, ANSI/ESDA/JEDEC JS-001-2024 | 3A |
| | Electrostatic discharge (Device Charging Model CDM) | TA = 25℃, ANSI/ESDA/JEDEC JS-002-2022 | C3 |

## 6.6.3 Latch-Up Electrical Characteristics

| Symbol | Parameter | Test condition | Class |
|---|---|---|---|
| LU | Static Latch-Up | JESD78F | Class IA ($T_A$ = +25℃) |

# 7. Package Dimensions

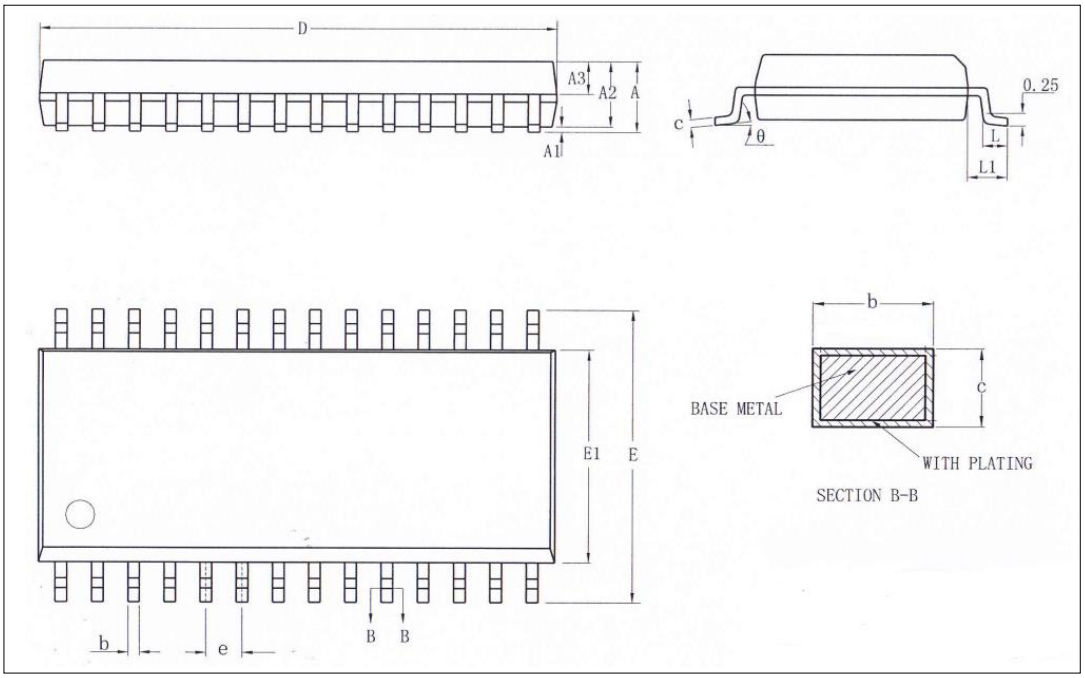
## 7.1 SOP20




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 2.65 |
| A1 | 0.10 | - | 0.30 |
| A2 | 2.24 | - | 2.44 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.39 | - | 0.47 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.25 | - | 0.30 |
| c1 | 0.24 | 0.25 | 0.26 |
| D | 12.65 | - | 12.90 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27BSC | | |
| h | 0.50REF | | |
| L | 0.70 | - | 1.01 |
| L1 | 1.40REF | | |
| θ | 0 | - | 8° |

Caution: Package dimensions do not include mold flash or gate burrs.

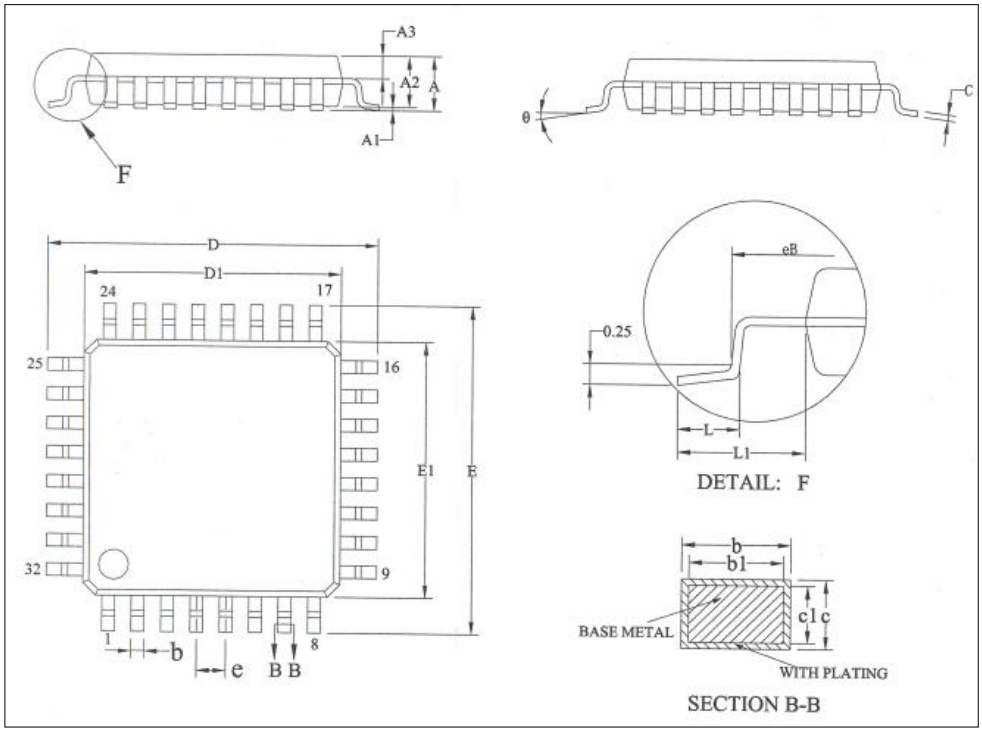
## 7.2 SOP28




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 2.65 |
| A1 | 0.10 | - | 0.30 |
| A2 | 2.24 | - | 2.44 |
| A3 | 0.97 | 1.02 | 1.07 |
| b | 0.39 | - | 0.47 |
| c | 0.25 | - | 0.30 |
| D | 17.90 | 18.00 | 18.10 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27BSC | | |
| L | 0.70 | - | 1.01 |
| L1 | 1.40REF | | |
| θ | 0 | - | 8° |

Caution: Package dimensions do not include mold flash or gate burrs.

## 7.3 LQFP32




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.32 | - | 0.43 |
| b1 | 0.31 | 0.35 | 0.39 |
| c | 0.13 | - | 0.18 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| eB | 8.10 | - | 8.25 |
| e | 0.80BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

Caution: Package dimensions do not include mold flash or gate burrs.

# 8. Revision History

| Version # | Date | Description of changes |
|---|---|---|
| V0.5.0 | Mar. 2025 | Initial release |
| V0.5.1 | Mar. 2025 | Modified DC electrical characteristics and output high/low voltage data |
| V0.5.2 | Jul. 2025 | 1) Modify the description of the function introduction section<br>2) Updated HSE test conditions in Section 6.3.2 External Oscillator. |